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## APPLICATION FOR LETTERS PATENT

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Methods of Forming Planarized Surfaces Over  
Semiconductor Substrates

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## Methods Of Forming Planarized Surfaces Over Semiconductor Substrates

### TECHNICAL FIELD

**[0001]** The invention pertains to methods of forming planarized surfaces over semiconductor substrates.

### BACKGROUND OF THE INVENTION

**[0002]** Numerous applications exist in semiconductor processing in which it is desired to form planarized surfaces over uneven topography. The planarized surfaces will typically not be absolutely planar in a mathematical sense, but rather will be approximately planar in that there can be minor variations across the surfaces which cause the surfaces to deviate from absolute planarity. Such minor variations can include, for example, dishing, which is a common occurrence if chemical-mechanical polishing (CMP) is utilized for the planarization of a surface. The term “substantially planar” is utilized herein to indicate that a surface has only minor variations from absolute planarity, with typical minor variations being within about +/- 5% from absolute planarity.

**[0003]** One method for forming a planarized surface is as follows. Initially, a single material is deposited over a non-planar topography. The material is deposited to a sufficient thickness so that the material completely covers and fills the non-planar topography of the substrate. An upper surface of the material will typically be non-planar as-deposited, in that the material will deposit over the non-

planar topography of the substrate with some conformality. The material is subsequently planarized with an appropriate process, such as, for example, chemical-mechanical polishing (CMP) to substantially planarize the upper surface of the material.

**[0004]** A problem with planarization of a single material is that it is difficult to ascertain an appropriate stop point within the material. For instance, if CMP is utilized, a rate of removal of the material by the CMP can be estimated, and the CMP can then be timed in an attempt to remove a desired thickness of the material. However, minor variations in temperature, type of slurry, polishing pad wear, etc. can impact the rate of removal of material by CMP. Accordingly, the rate of removal of the material by the CMP can vary as the various components utilized in the polishing process age, and/or if temperature varies. This can make it difficult to control CMP processes within the tight tolerances desired for modern semiconductor device processing.

**[0005]** If the CMP process is not appropriately maintained within desired tolerances, there can be a non-uniform thickness of material across the substrate after the CMP, which can create difficulties in fabrication steps following the CMP.

**[0006]** It is desired to develop new methods for forming planarized surfaces over semiconductor substrates to alleviate the problems discussed above.

## SUMMARY OF THE INVENTION

**[0007]** In one aspect, the invention encompasses an observation that a spin-on-dielectric (SOD) can typically be deposited with better uniformity than a timed CMP process can achieve. In such aspect, the invention encompasses methods for improving post-CMP thickness uniformity across a semiconductor wafer by utilizing an SOD as a polish stop.

**[0008]** In one aspect, the invention encompasses a method of forming an electrically insulative surface over a semiconductor substrate. A substrate is initially provided to have a substantially non-planar surface topography. A SOD material is formed over the substantially non-planar surface topography of the substrate. A second dielectric material is formed over the SOD material. The second material is polished while using the SOD material as a polishing stop. The polishing utilizes conditions which remove the second dielectric material at a faster rate than the SOD material. The polishing forms an electrically insulative surface over the semiconductor substrate, with such surface comprising both the SOD material and the second dielectric material.

**[0009]** In one aspect, the invention encompasses a method of forming a planarized surface over a memory array region and a peripheral region of a semiconductor substrate. The memory array region has a different average elevational height than the peripheral region. Polysilazane is formed over the memory array region and over the peripheral region. At least a portion of the

polysilazane is densified. A material is formed over the polysilazane. The material has a different average elevational height over the memory array region than over the peripheral region. The material is planarized under conditions which remove the material at a faster rate than the densified polysilazane. The planarizing forms a planarized surface which comprises the polysilazane and the material, and which extends over the memory array and peripheral regions.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]** Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

**[0011]** Fig. 1 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment at a preliminary processing stage of an exemplary aspect of the present invention.

**[0012]** Fig. 2 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 1.

**[0013]** Fig. 3 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 2.

**[0014]** Fig. 4 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 1 in accordance with an aspect of the invention alternative to that of Fig. 2.

**[0015]** Fig. 5 is a view of the Fig. 1 wafer fragment shown at a processing stage subsequent to that of Fig. 4.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0016]** This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

**[0017]** An exemplary aspect of the invention is described with reference to Figs. 1-3. Referring initially to Fig. 1, a fragment 10 of a semiconductor wafer is illustrated at a preliminary processing stage. Fragment 10 comprises a base 12 which can comprise, consist essentially of, or consist of monocrystalline silicon lightly-doped with background p-type dopant.

**[0018]** To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. In accordance with such definition of "substrate", the

structure 12 can itself be a substrate, or the combination of structure 12 with various other structures can be a substrate.

**[0019]** Base 12 is divided into a pair of regions 14 and 16. A plurality of structures 18 are shown formed over region 14 and not over region 16. The shown structures 18 are separated from one another by gaps 20. The structures 18 and base 12 can be together considered a semiconductor substrate in some aspects of the invention. Such semiconductor substrate has a substantially non-planar surface topography. Specifically, features 18 correspond to projections of the substrate separated by gaps 20, and accordingly correspond to non-planar regions of the substrate.

**[0020]** The structures 18 increase an average elevational height of the semiconductor substrate within region 14 relative to an average elevational height of the substrate within region 16. Structures 18 can have elevational heights of greater than or equal to about 1000Å, with a typical height being from about 1000Å to about 3000Å. The difference in the average elevational height associated with region 14 relative to the average elevational height associated with region 16 can thus be greater than 1000Å, and in some aspects of the invention can be from about 1000Å to about 3000Å.

**[0021]** Structures 18 are diagrammatic representations of features associated with semiconductor substrate 12. The structures 18 can comprise any suitable material or combination of materials, and can comprise any suitable shapes. In

particular aspects of the invention, region 14 is a memory array region of a semiconductor substrate, and accordingly structures 18 can correspond to features associate with a memory array. For instance, structures 18 can correspond to capacitor structures and/or transistor structures associated with a dynamic random access memory (DRAM) array.

**[0022]** Region 16 is peripheral to the memory array and can comprise various logic circuit elements (not shown) and/or other integrated circuit devices. It is to be understood that regions 14 and 16 can be reversed. Accordingly, the memory array region can have an average elevational height associated therewith which is less than the average elevational height associated with the peripheral region, or vice versa.

**[0023]** Although base 12 is shown as a single homogeneous composition, it is to be understood that base 12 can comprise numerous layers of integrated circuitry at various processing stages, and that the methodology of the invention can be utilized at any suitable processing stage. Accordingly, methodology of the present invention can be utilized at a processing stage in which base 12 corresponds to a single homogeneous composition of bulk semiconductor material, and/or can be utilized at one or more processing stages in which base 12 comprises multiple layers of integrated circuitry. Also, although all of the structures 18 are shown having the same height as one another and the same general shape as one another, it is to be understood that the structures 18 can differ in height and/or



shape relative to each other, and can also differ in composition relative to each other.

**[0024]** Referring to Fig. 2, a spin-on-dielectric (SOD) 22 is formed over regions 14 and 16 of the semiconductor substrate comprising base 12 and structures 18. The SOD is somewhat conformal to the non-planar surface of the substrate, and accordingly has a greater average elevational height over region 14 of the substrate than over region 16 of the substrate.

**[0025]** The SOD can comprise any suitable material, and in particular aspects will comprise, consist essentially of, or consist of silicon, nitrogen and hydrogen. For instance, the SOD can comprise, consist essentially of, or consist of polysilazane. If polysilazane is used, such can be densified after it is spun over the substrate. The densification converts the polysilazane partially or fully into a silicon dioxide. The densification can comprise steam densification at a temperature of from about 350°C to about 1000°C, with about 600°C being typical. The densification time can be from about 15 minutes to about 2 hours, with about 30 minutes being typical. The densification will proceed from the top of SOD material 22 to the bottom of the material. The densification can be conducted to proceed entirely through the SOD layer, or can be conducted to treat only the upper portion of the layer. In particular aspects, the SOD layer 22 will have an average thickness, and the treatment will be conducted so that only the upper 50% of the average thickness is treated, in other aspects only the upper 75% of the average thickness is

treated, and in yet other aspects the entirety of the thickness is treated with the densification process.

**[0026]** The thickness of the SOD material 22 is preferably such that the material is thicker than the tallest feature 18 is high. Accordingly, if features 18 extend to a height of 3000Å, the SOD layer will be formed to a thickness greater than 3000Å.

**[0027]** A second material 24 is formed over SOD material 22. Second material 24 can have a thickness greater than or equal to the thickness of SOD material 22, and accordingly in particular aspects of the invention will have a thickness exceeding 3000Å. Second material 24 can be a dielectric material (i.e., an electrically insulative material), and in particular aspects will comprise, consist essentially of, or consist of doped silicon oxide, with an exemplary suitable doped silicon oxide being borophosphosilicate glass (BPSG). The second material 24 has a non-planar surface topography, in that the second material is formed substantially conformally over SOD material 22. The second dielectric material 24 thus has a different average elevational height over the region 14 than over the region 16. Second material 24 can be formed by any suitable method, including, for example, chemical vapor deposition.

**[0028]** The above-described densification of SOD material 22 can occur before, after or during formation of the second material 24.

**[0029]** Referring to Fig. 3, material 24 is planarized while using material 22 as a stop. The planarization can remove some of material 22 while removing material 24, but removes material 24 at a faster rate than the material 22 so that the planarizing slows down upon reaching material 22. The planarization can be accomplished utilizing, for example, chemical-mechanical polishing, and accordingly material 22 can be considered a polishing stop. The term “polishing stop” is utilized to indicate that the polishing slows upon reaching material 22, which includes, but is not limited to, applications in which the polishing comes to a complete stop upon reaching material 22. Typically, the polishing process will not come to a complete stop upon reaching material 22, but will slow substantially. In some aspects, material 24 can be considered “softer” than material 22 under particular polishing conditions in that material 24 is removed more rapidly than material 22 during the polishing.

**[0030]** If material 24 comprises, consists essentially of, or consists of BPSG and material 22 comprises, consists essentially of, or consists of one or both of polysilazane and silicon dioxide formed from exposure of polysilazane to densification conditions, a suitable polishing process for removing material 24 relative to material 22 is a CMP process. The CMP process can utilize a polishing pad pressure of greater than 0 psi and less than or equal to about 10 psi, an uncontrolled temperature (which will typically be about room temperature), and a slurry composition comprising cerium oxide and a surfactant. The cerium oxide can

be present to a concentration of from about 0.2% to about 1.5%, by weight. A suitable polishing pad is a pad comprising polyurethane. A suitable pad hardness is from about 45 Shore D to about 60 Shore D. The pad hardness can impact the extent to which dishing occurs. Specifically, if a pad is suitably hard, dishing can be substantially avoided.

**[0031]** Fig. 3 shows that the polishing forms a surface 30 which extends across materials 22 and 24, and which is substantially planar. Surface 30 can, in particular aspects, have a bit of dishing occurring over material 24 due to the polishing of material 24 being somewhat faster than the polishing of material 22. Surface 30 has a portion over region 16 which primarily comprises material 24, and another portion over region 14 which primarily comprises material 22. Typically, materials 22 and 24 will both be electrically insulative materials, and accordingly surface 30 will be an electrically insulative surface.

**[0032]** As was indicated above, the structures 18 associated with region 14 can be memory device structures, and accordingly region 14 can correspond to a memory array. Region 16 can thus correspond to a portion of the substrate peripheral to the memory array. As was also mentioned above, the memory array region and peripheral region can be reversed such that the structures are associated with a peripheral region 14 and the memory array region is associated with the relatively flat portion 16 at the processing stage of Figs. 1-3. Typically, however, the memory array region will have the relatively non-planar features 18

associated therewith (i.e., the region 14 will correspond to the memory region), and the region peripheral to the memory array region will have much smaller structures associated therewith (and accordingly the region 16 will correspond to the region peripheral to the memory array region).

**[0033]** Figs. 1-3 illustrate one aspect of the invention. Another aspect is described with reference to Figs. 4 and 5. In referring to Figs. 4 and 5, identical numbering will be used as was used above in describing Figs. 1-3, where appropriate.

**[0034]** Fig. 4 shows the fragment 10 at a processing stage subsequent to that of Fig. 1, and specifically shows the SOD material 22 and second material 24 formed over a substrate comprising base 12 and features 18. A difference between the structure of Fig. 4 and that of Fig. 1 is that the SOD material 22 has flowed conformally into the gaps 20 between structures 18 to form a wavy surface 31 over region 14. Wavy surface 31 can result if gaps 20 have a relatively low critical dimension, and the structure of Fig. 2 can result if the gaps 20 have a higher critical dimension.

**[0035]** Referring to Fig. 5, material 24 is planarized to form a substantially planar upper surface 40. A difference between the upper surface 40 of Fig. 5 and the substantially planar upper surface 30 of Fig. 3 is that the upper surface 40 comprises several domains of material 24 over region 14, whereas the upper

surface 30 consisted only of material 22 over the structures 18 and gaps 20 (Figs. 2 and 4) associated with the region 14.

**[0036]** Either of the structures of Fig. 3 or Fig. 5 can be suitable for semiconductor applications. Specifically, the structures of Figs. 3 and 5 have substantially planar surfaces 30 and 40 which can be subsequently utilized as base surfaces for forming additional layers of circuitry over the underlying substrate comprising structures 12 and 18.

**[0037]** An advantage of the present invention relative to prior art processes is that the invention can enable accurate control of the thickness of material remaining over region 14 after a polishing process. Specifically, the polishing process has a defined endpoint corresponding to the surface of material 22. A CMP process can be monitored by any of numerous methods (including, for example, monitoring the friction of a CMP process, optically monitoring the residue generated during a CMP process, etc.) to determine when such endpoint has been reached. In prior art processes in which the polishing time was utilized to determine the thickness of a remaining material, a parameter of the CMP stage was utilized alone to control the thickness of the remaining material (specifically, the duration of the CMP process). In contrast, the present invention utilizes one or more parameters of the deposition stage utilized for formation of SOD 22 (specifically, parameters utilized to fix the thickness of material 22) to control the thickness of material remaining after the CMP process. The present invention can thus allow tighter tolerances to be

obtained relative to the thickness of the material remaining after a polishing process than can be obtained utilizing prior art processes.

**[0038]** Processing of the present invention can improve numerous facets of fabrication processes. For instance, if a dry etch is utilized to form contact openings through either planarized surface 30 (Fig. 3) or planarized surface 40 (Fig. 5) the etch depth will be consistent from lot to lot relative to prior art processes, from wafer to wafer, and from die to die, which can improve electrical properties of functional semiconductor assemblies because the uniformity from one assembly to another will be more consistent. This can also improve the yield of semiconductor fabrication processes utilizing the present invention relative to prior art processes.

**[0039]** In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.